C-SHAPED DDR PHY IP LAYOUT

Challenges & Custom Methodology

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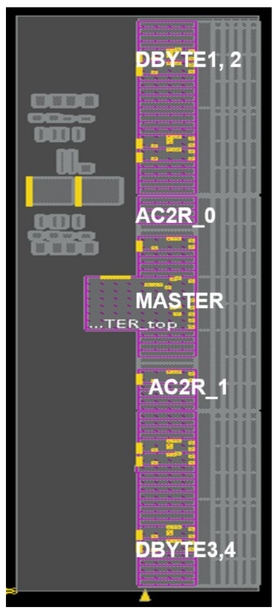
1. BACKGROUND

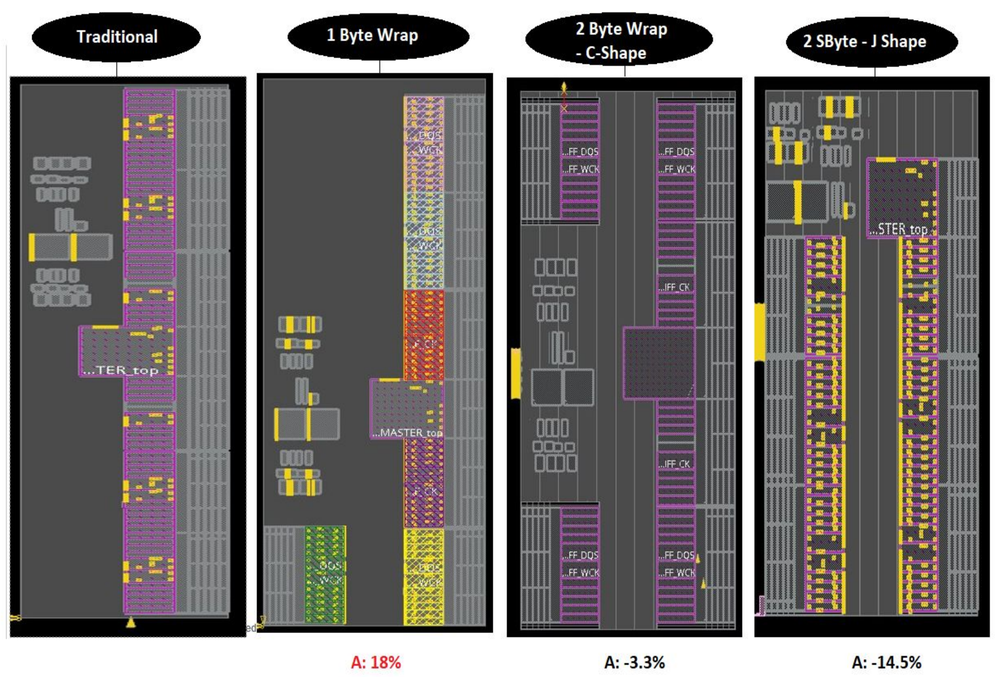
- IO IPs are traditionally designed to be placed along the chip edge for easiest integration on both die and package.
- Many IPs are no longer monolithic PHYs, and instead provided as a set of building blocks that are put together in Physical Design to allow for many different configurations with the same set of pieces.
- This opens up opportunities to optimize integrated IP area with creative floorplans.
  - –Need to keep IP integration rules in mind as we bend and potentially break them.

2. TRADITIONAL APPROACH

- **IP is designed for layout along chip edge.**
  - –Easy layout / stacking of PHY components.
  - –Bits /mm of edge space is low and can quickly become a bound-on die size.
  - –Hard to effectively use floorplan space in IP-integrating block. Corner areas will generally end up being dead space.
- **Opportunity to “wrap around” PHY components.**
  - –Reduce edge space.
  - –Better utilize block floorplan area.
- **Consider multiple alternate layouts:**
  - –Wrap around 1 component – save height, but not area efficient.
  - –Wrap around 2 components – save height and start saving area.
  - –Wrap around 3 components – save height and save considerable area, but bit density getting too high.

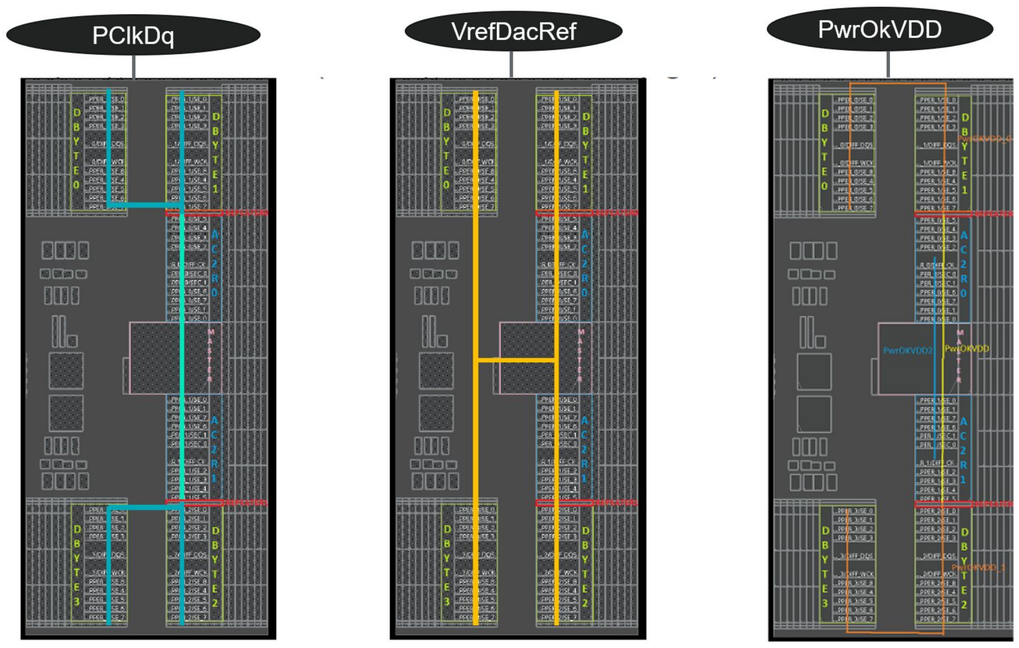


3. LAYOUT OPTIONS



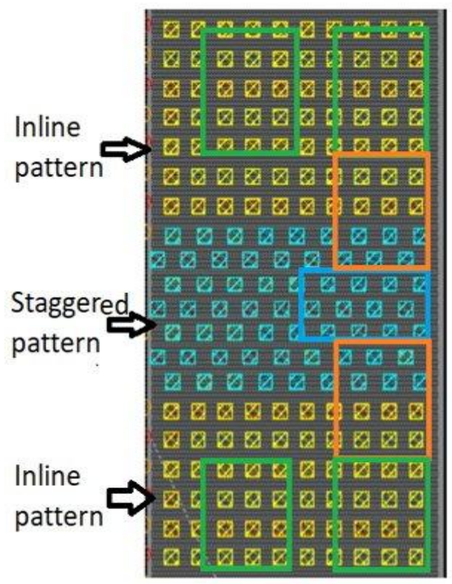
4. COMMON NET STITCHING

- PHY pieces include common nets (clk, ref, etc) that must be connected.
- In a linear layout, these easily stitch together.
- With a wrapped layout, more complex routing topologies are required.
  - –Need to take care with length / via limits; violations require spice simulation.



5. BUMP PLANNING

- **Inline bump pattern:**
  - –Can be package friendly when bumps share nets horizontally.
  - –Worst IR drop due to increased bump spacing.
  - –Easier straight-line RDL routing from IP to bump.
- **Staggered bump pattern:**
  - –More complex package routing required.
  - –Better IR drop due to decreased bump spacing.
- **Hybrid solution:**
  - –Staggered pattern over central area where most digital logic is placed (IR more critical)
  - –Inline pattern over top/bottom PHY areas (bump routing more critical)



6. CONCLUSION

- IPs being delivered as a set of building blocks that are put together in a certain configuration in Physical Design provides unique opportunities to optimize the floorplan to better utilize chip space.
- Significant edge and area savings are possible with optimized floorplans.
- Rules for integration are generally designed for placement along chip edge, so need to take care as rules are bent or broken in a custom implementation.
  - –Rules for custom routing stitching PHY pieces together.
  - –Impact to package routing with denser / more inset bumps.